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GALILEO GEN2

INTEL QUARK X1000

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PB: H48142-207

PBA: H48125-800

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Thu Sep 11 08:52:51 2014

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		
TITLE	GALILEO Gen2	DOCUMENT NUMBER
	DESIGN TITLE PAGE	H38681
		REV
		2.0
SHEET 1 OF 28		

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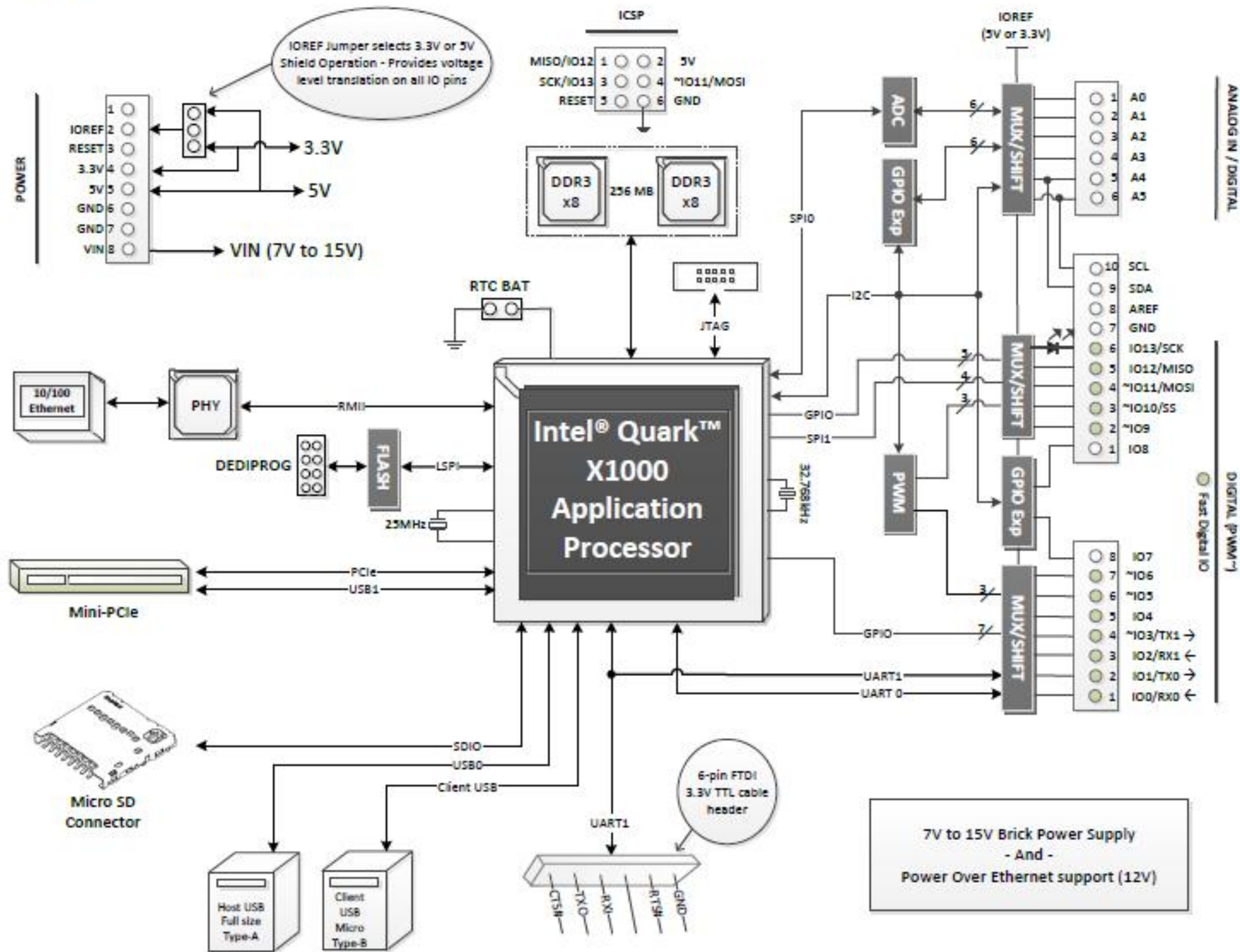
Intel® Galileo Design Document

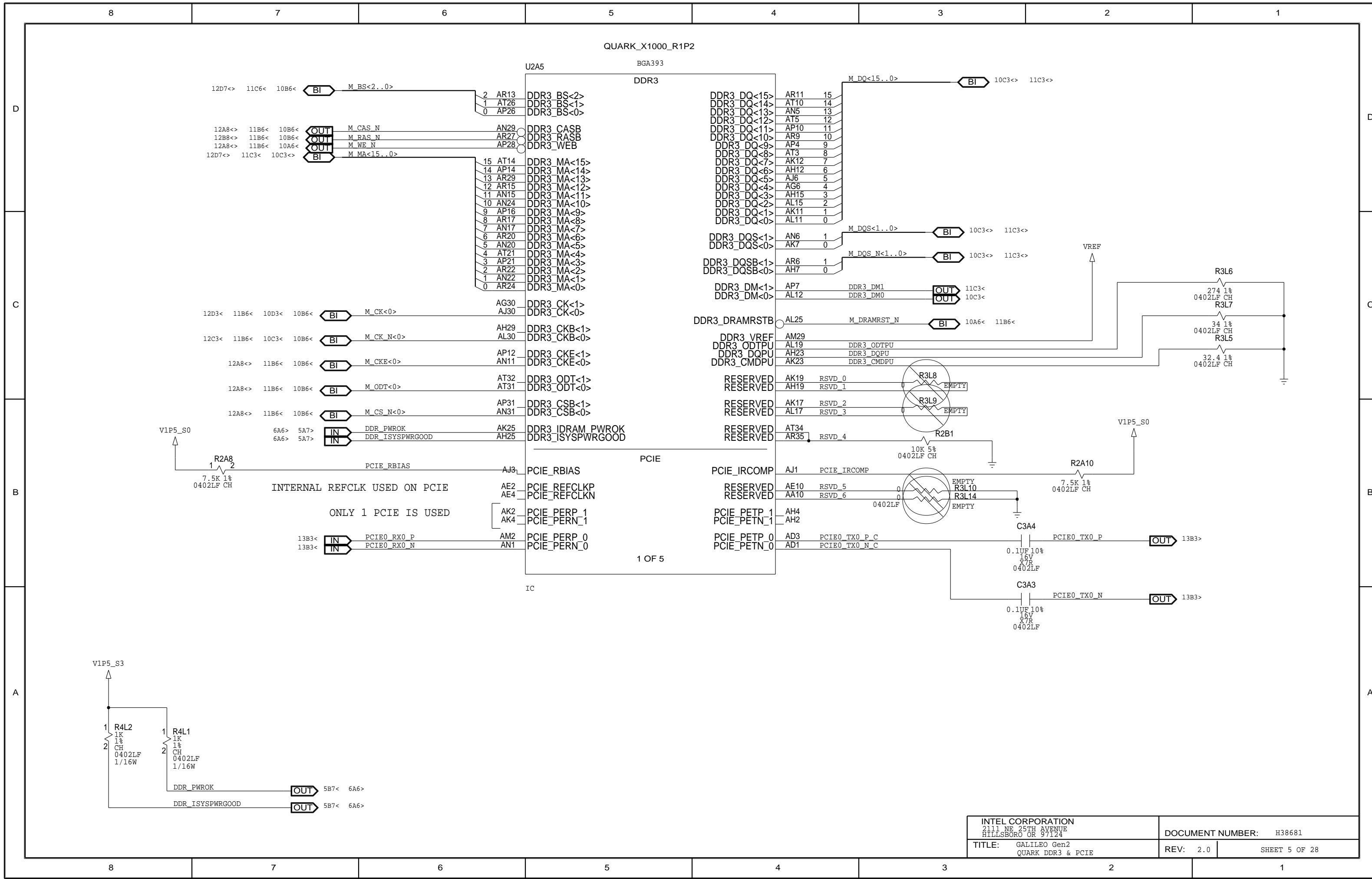
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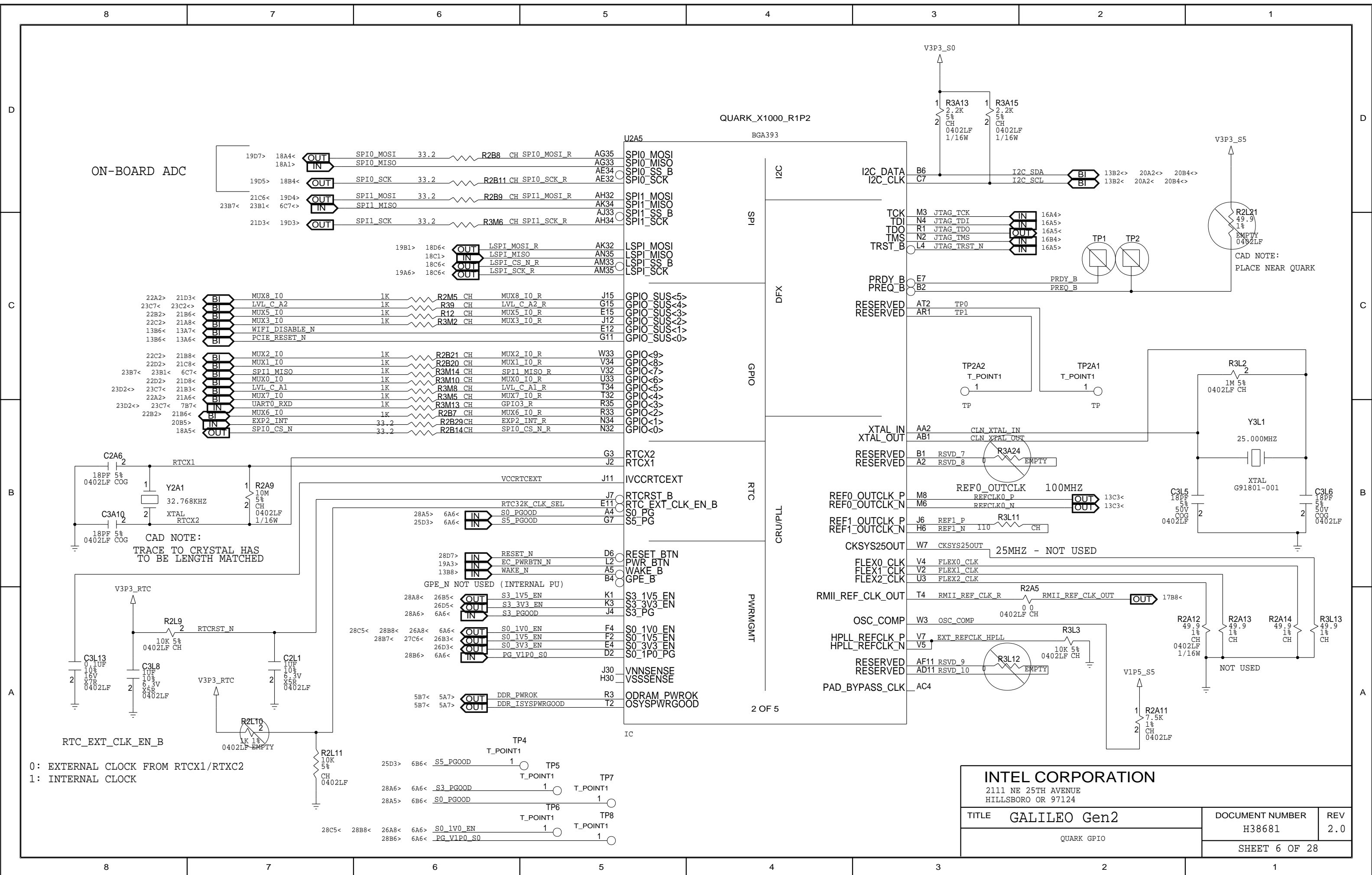
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INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 DISCLAIMER		REV: 2.0	SHEET 3 OF 28

Intel® Galileo™ Board Fab H (PVT)
May/2014

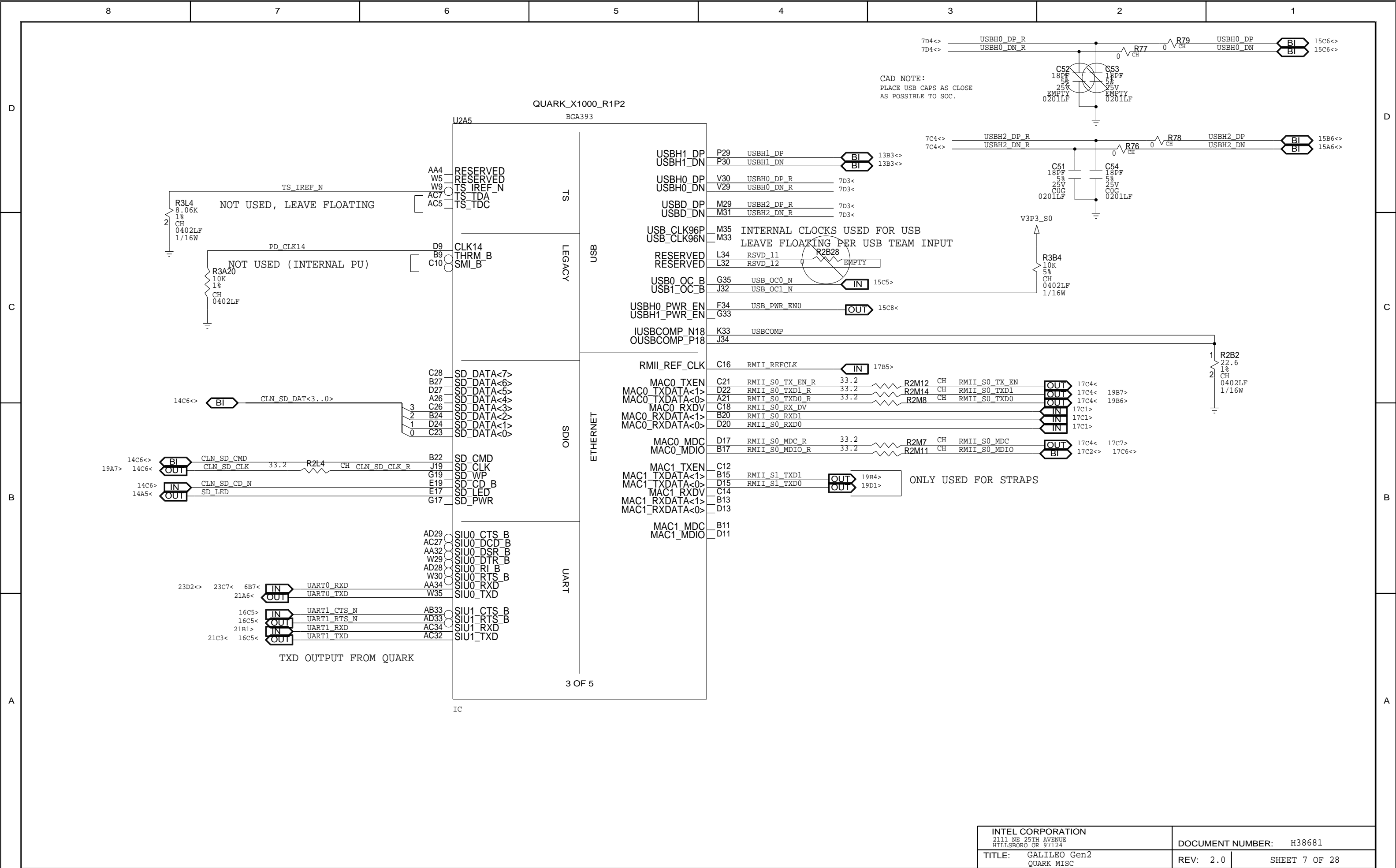






INTEL CORPORATION
 2111 NE 25TH AVENUE
 HILLSBORO OR 97124

TITLE	GALILEO Gen2	DOCUMENT NUMBER	H38681	REV	2.0
QUARK GPIO			SHEET 6 OF 28		



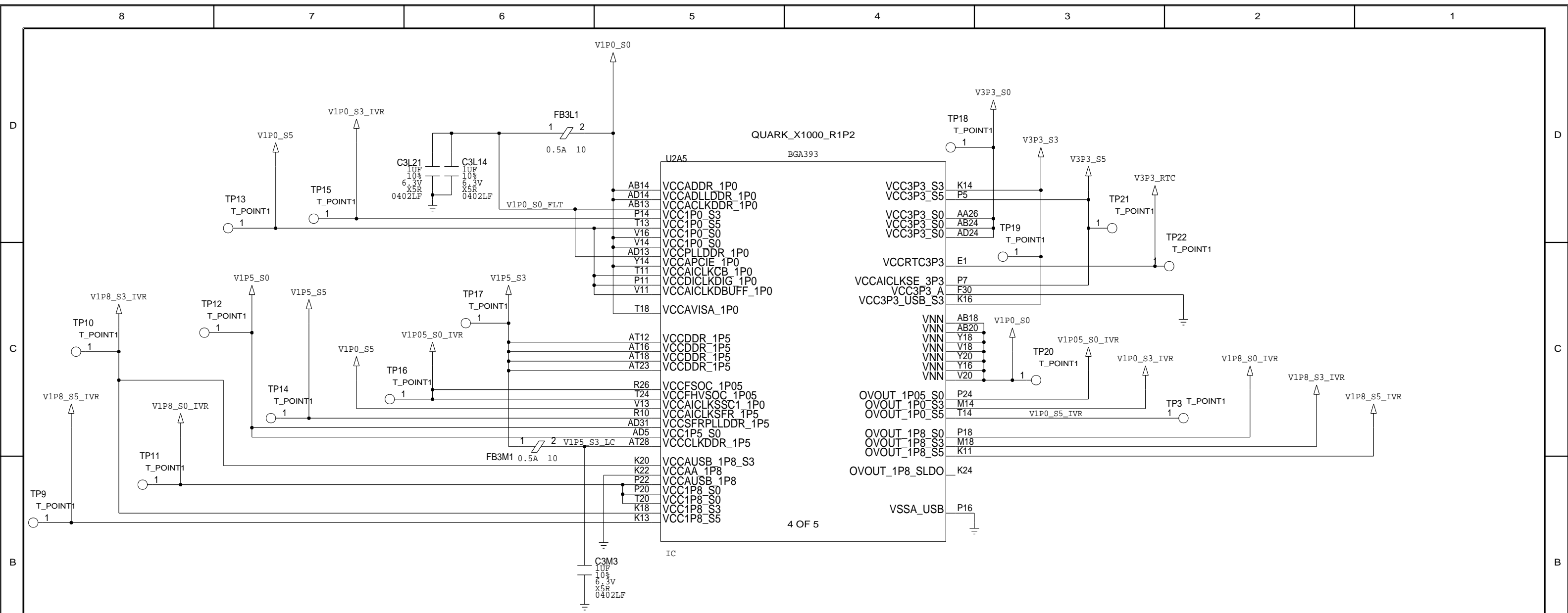
CAD NOTE:
PLACE USB CAPS AS CLOSE
AS POSSIBLE TO SOC.

INTERNAL CLOCKS USED FOR USB
LEAVE FLOATING PER USB TEAM INPUT

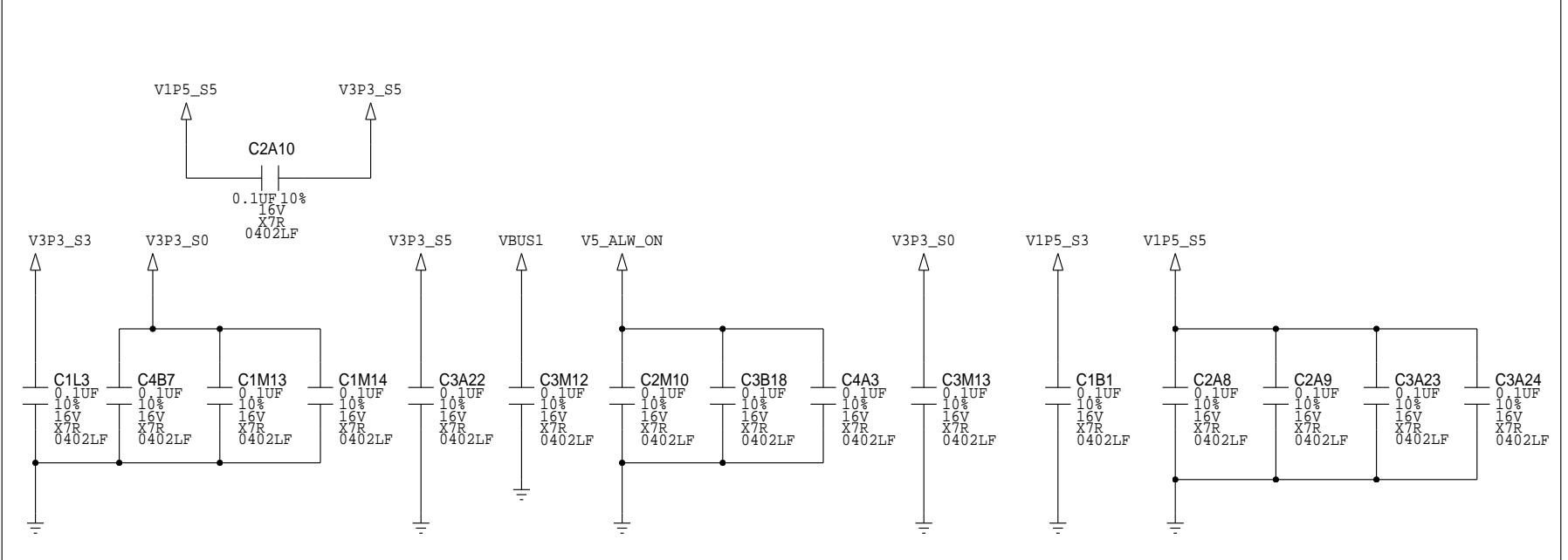
ONLY USED FOR STRAPS

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INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124			DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 QUARK MISC		REV: 2.0	SHEET 7 OF 28	

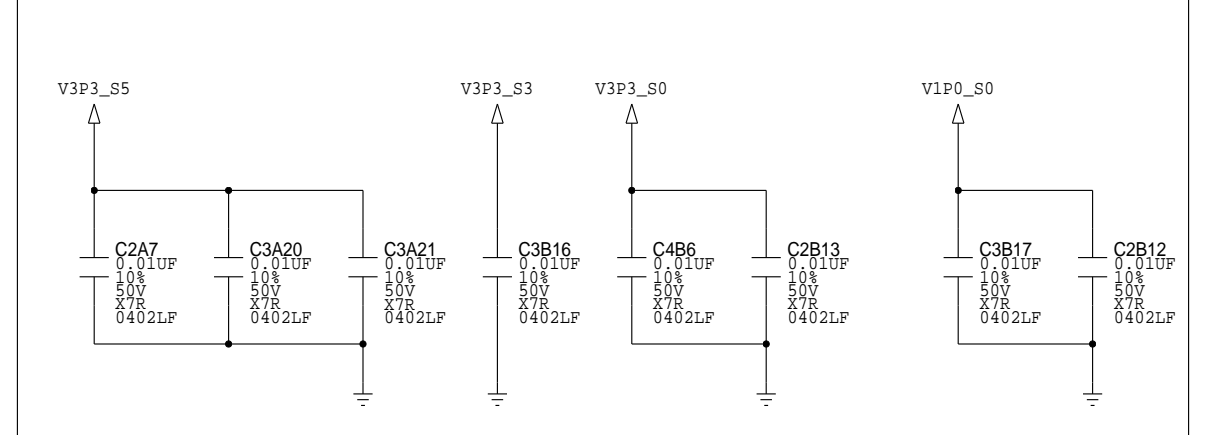


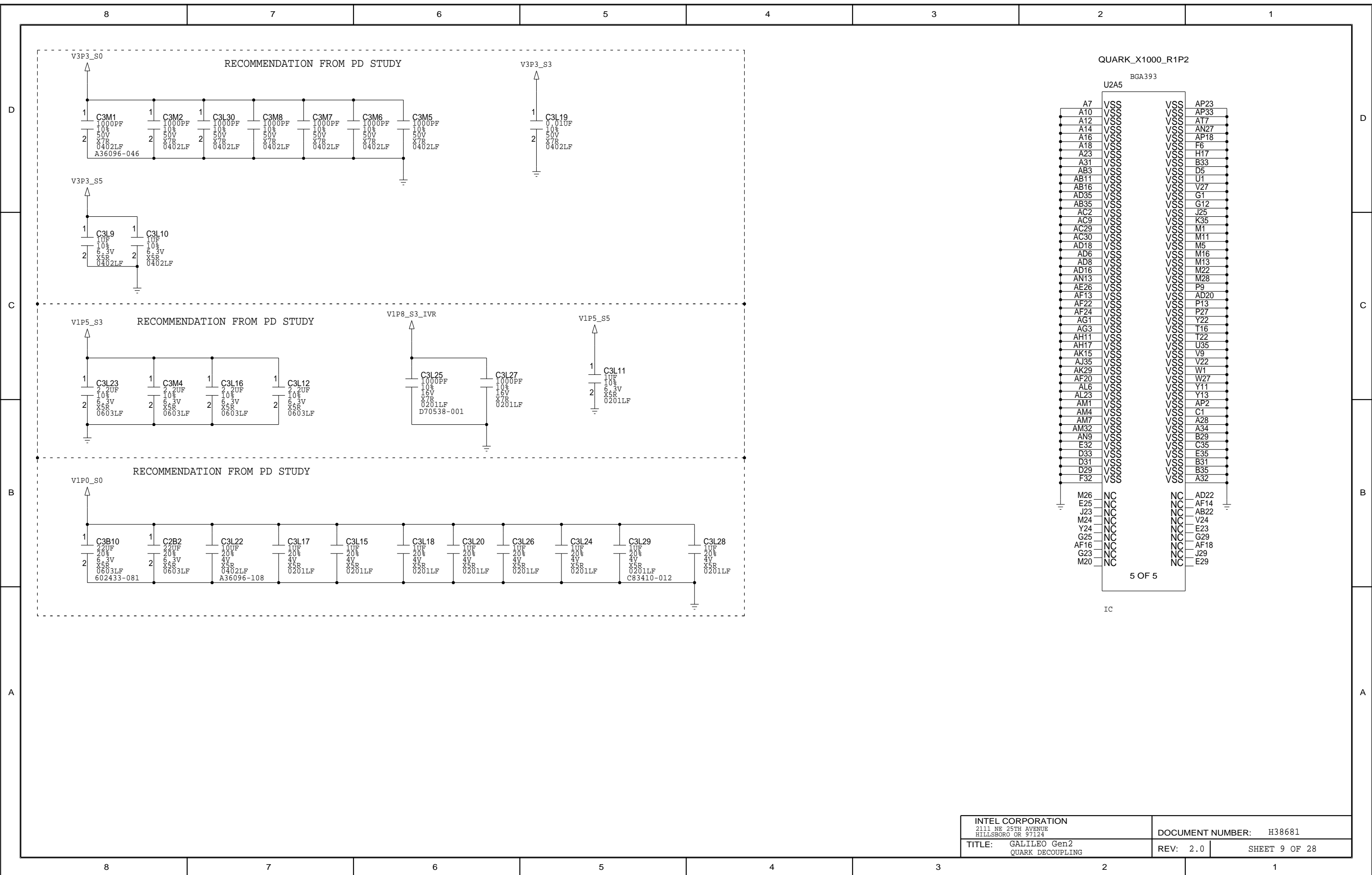
STITCHING CAPS FOR SPLIT PLANES

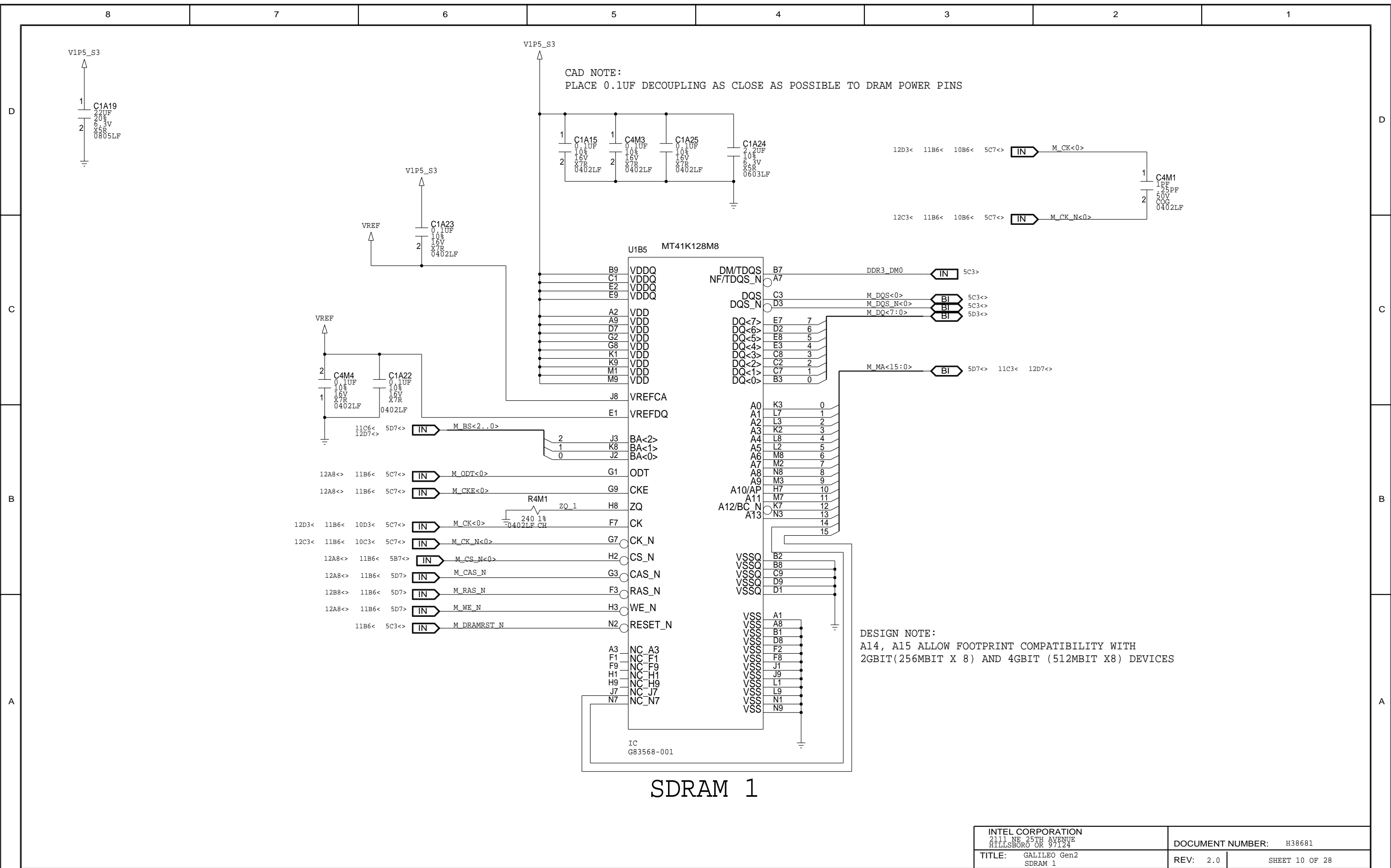


CAD NOTE
PLACE AS CLOSE AS POSSIBLE TO SIGNAL VIAS

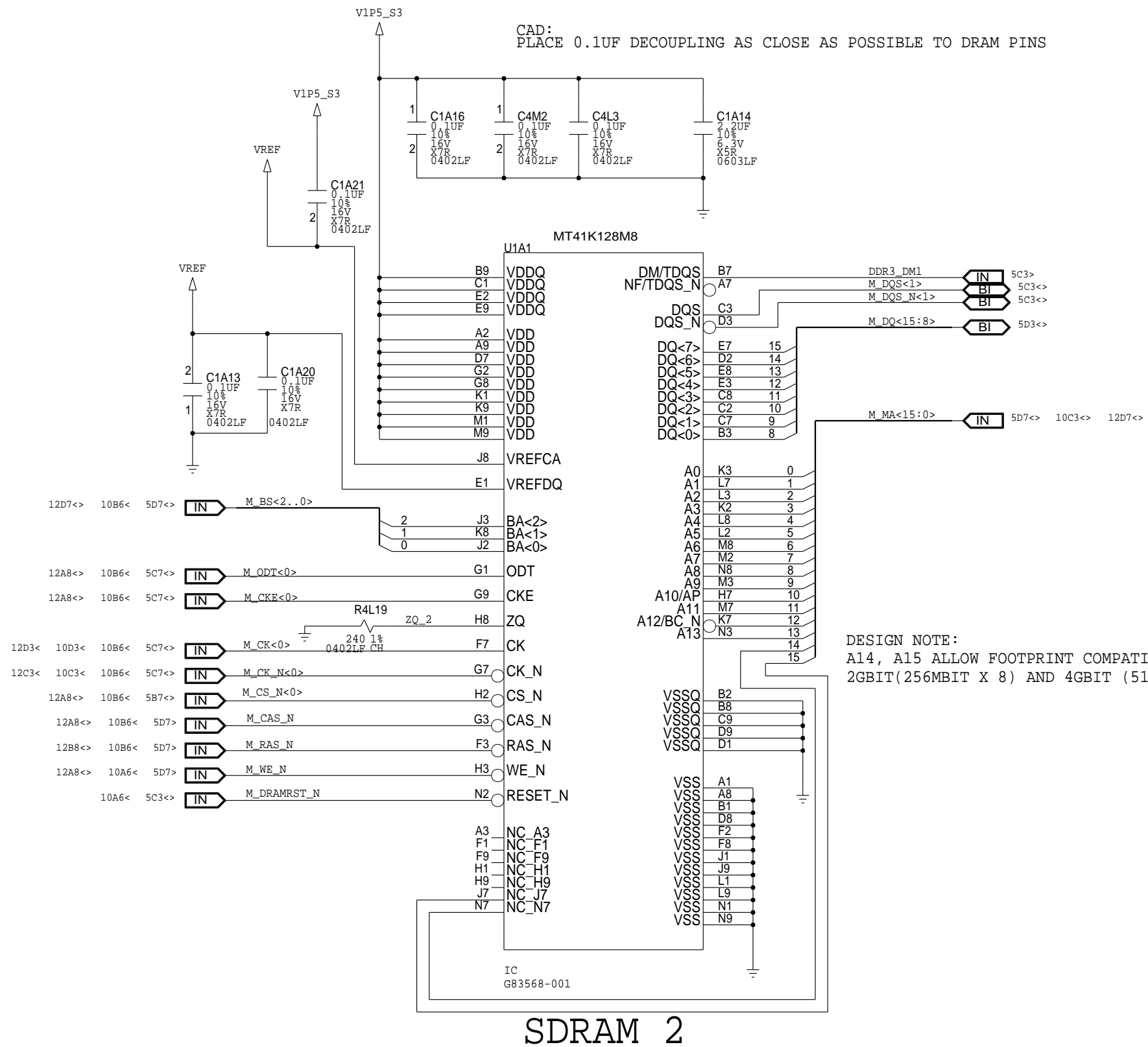
STITCHING CAPS FOR SIGNAL REFERENCE TRANSITION

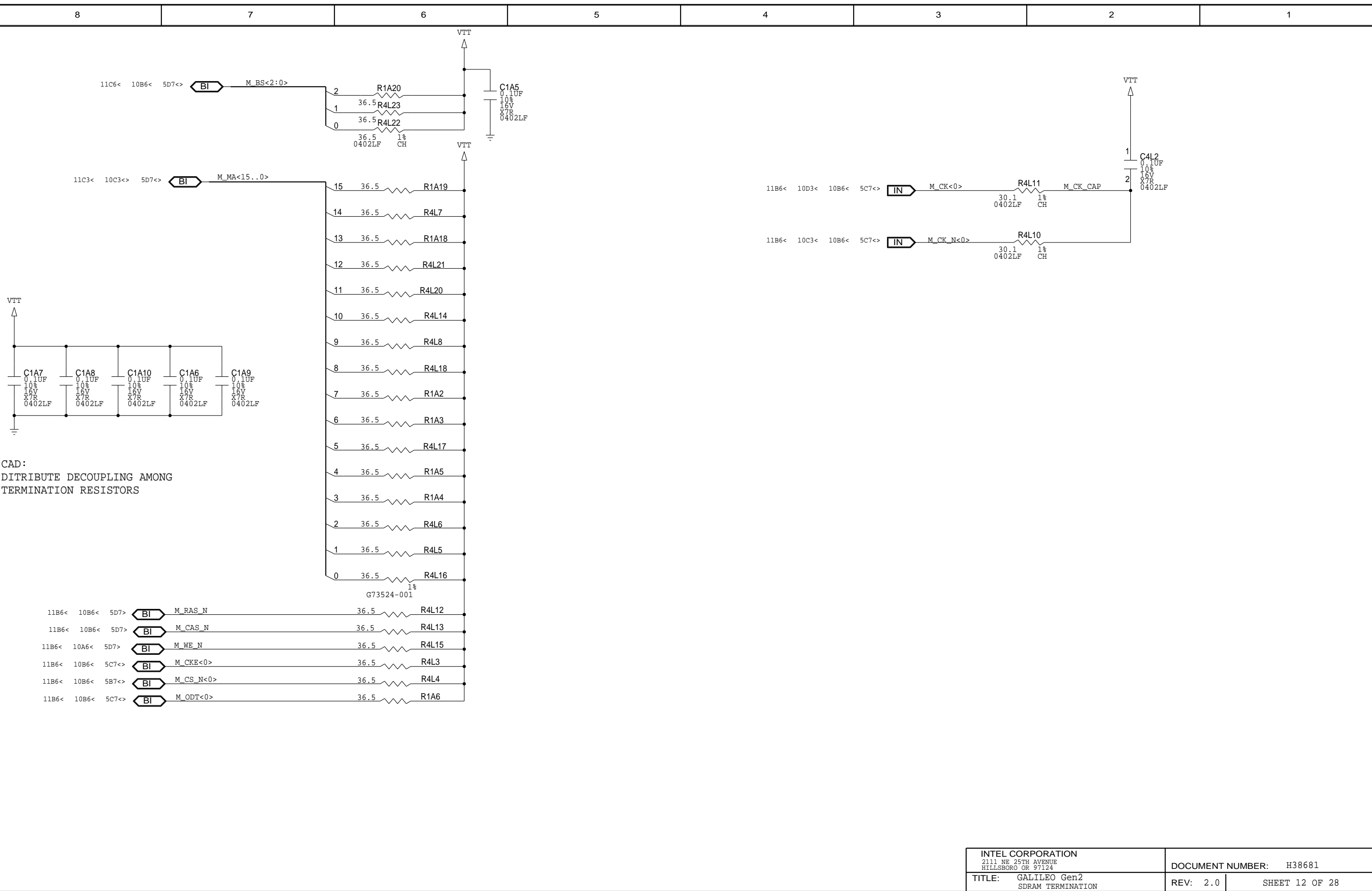


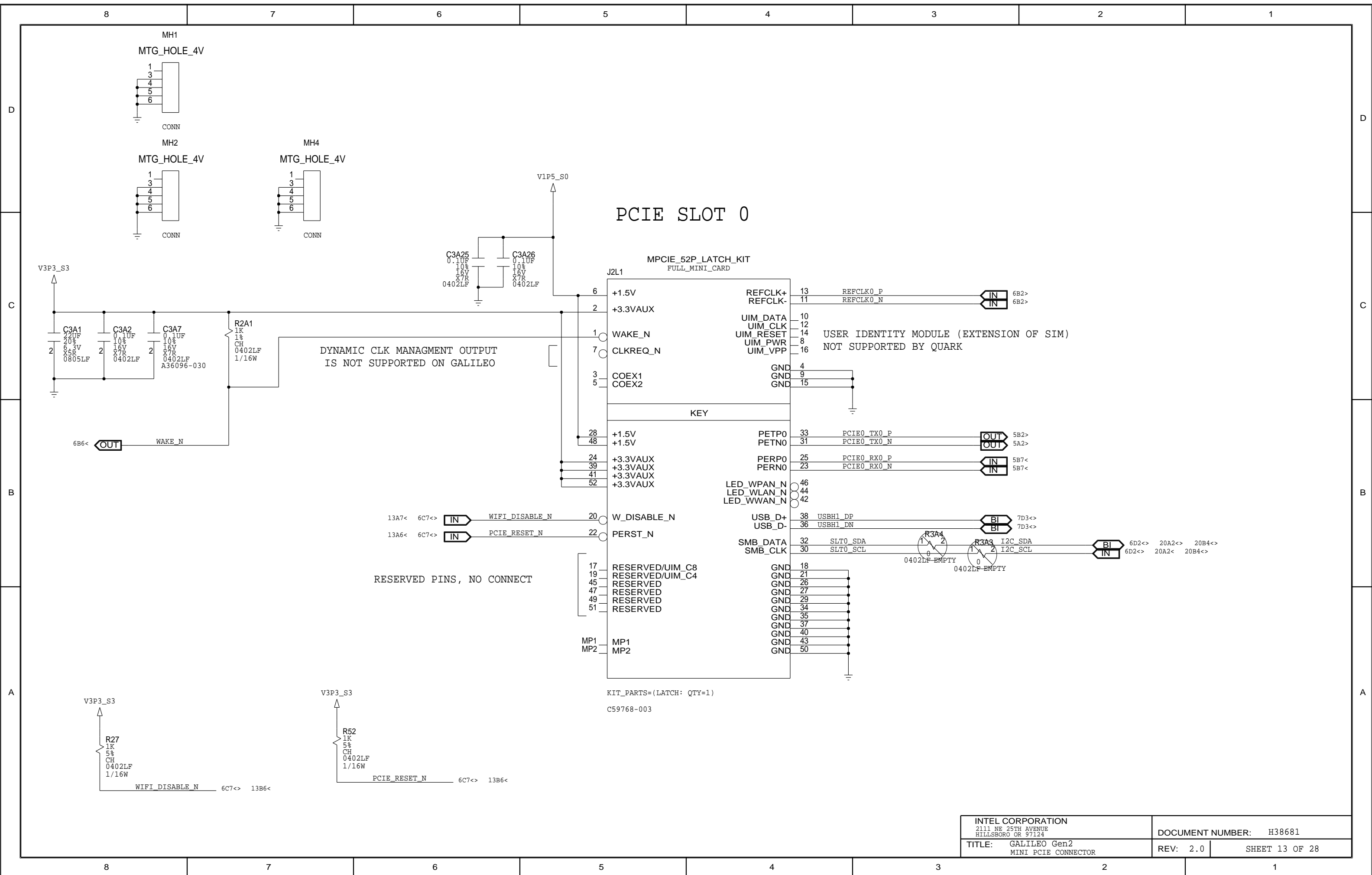




INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 SDRAM 1		REV: 2.0	SHEET 10 OF 28







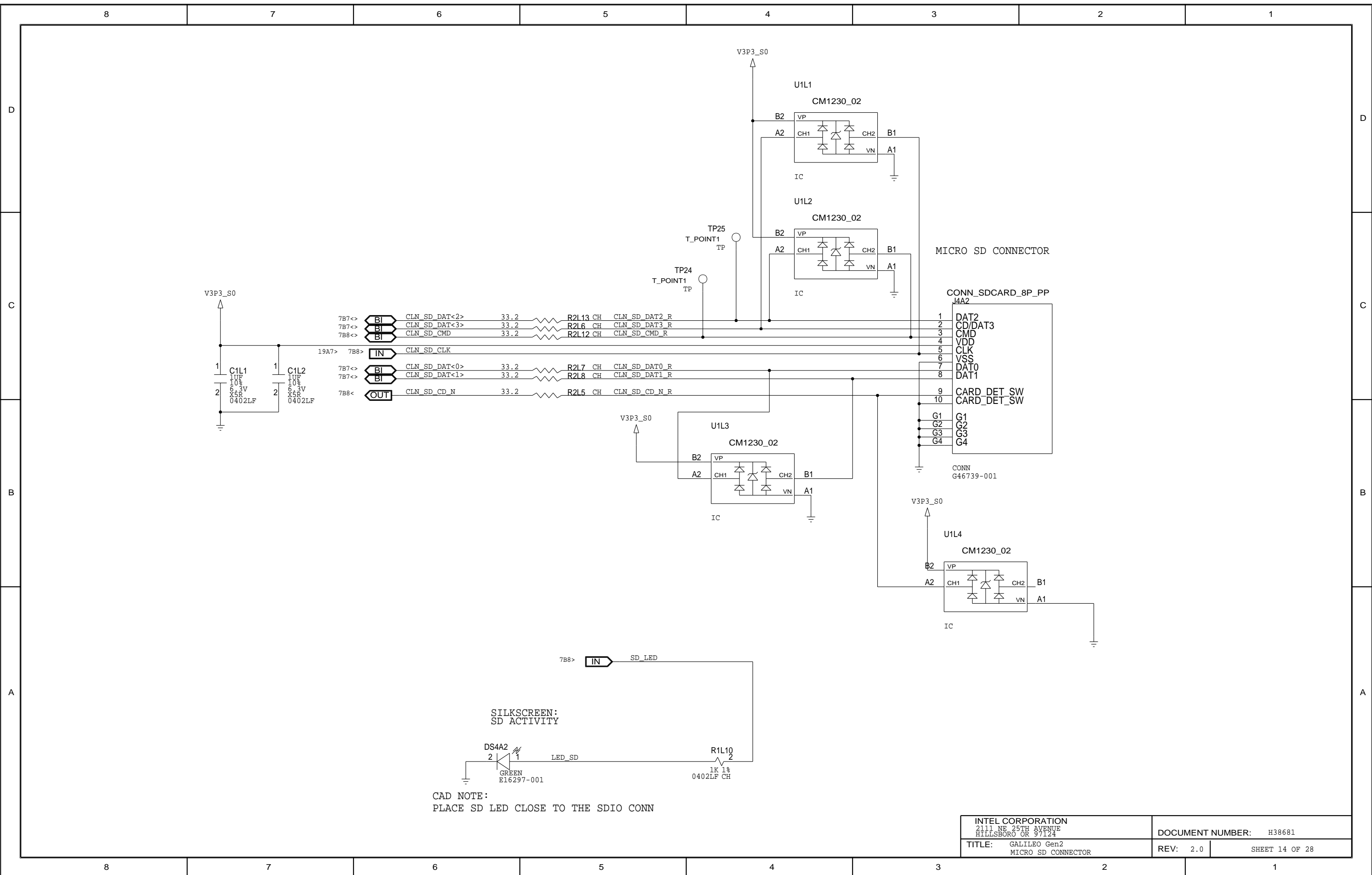
DYNAMIC CLK MANGAMENT OUTPUT
IS NOT SUPPORTED ON GALILEO

RESERVED PINS, NO CONNECT

USER IDENTITY MODULE (EXTENSION OF SIM)
NOT SUPPORTED BY QUARK

KIT_PARTS=(LATCH: QTY=1)
C59768-003

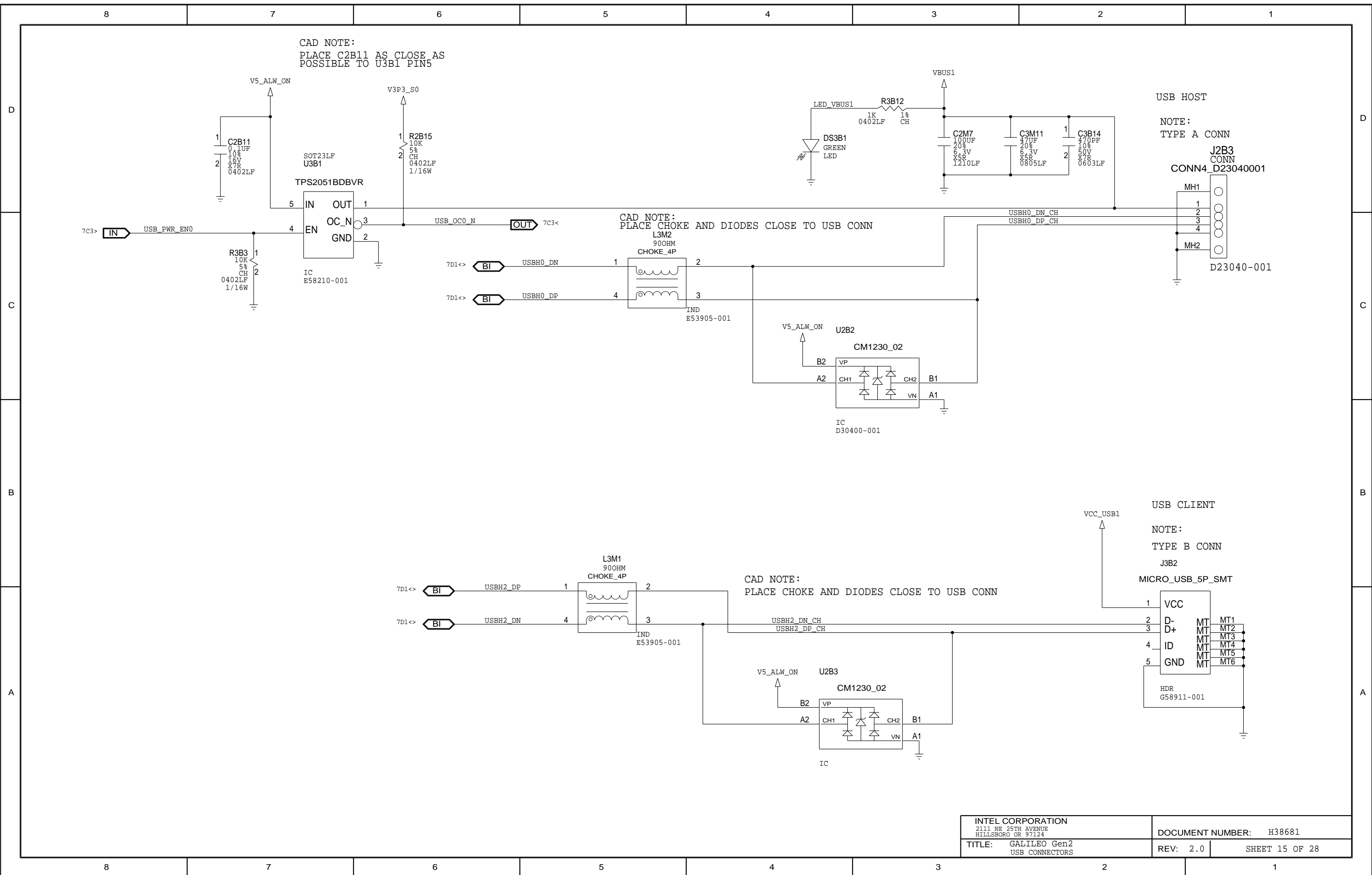
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 MINI PCIE CONNECTOR		REV: 2.0	SHEET 13 OF 28

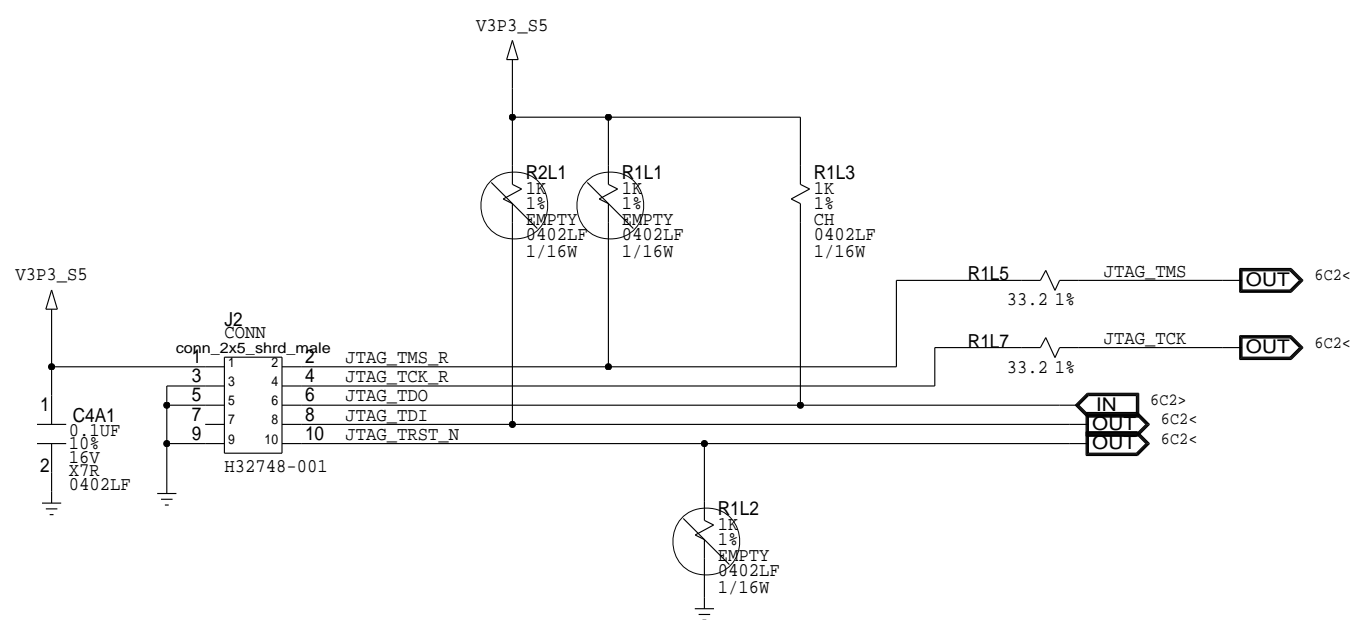
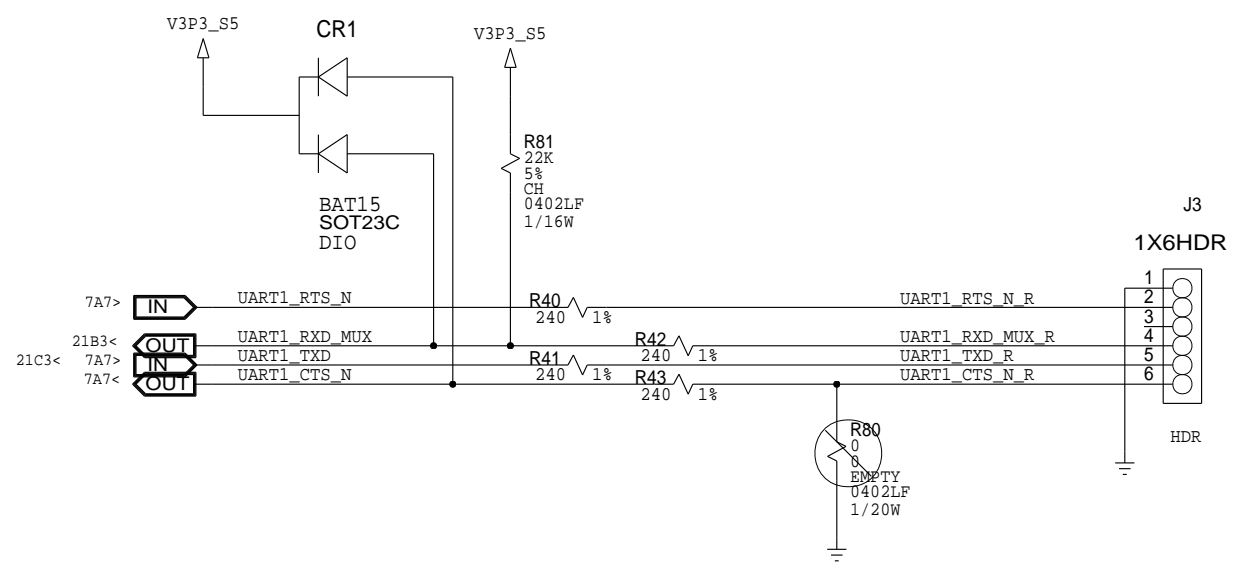


SILKSCREEN:
SD ACTIVITY

CAD NOTE:
PLACE SD LED CLOSE TO THE SDIO CONN

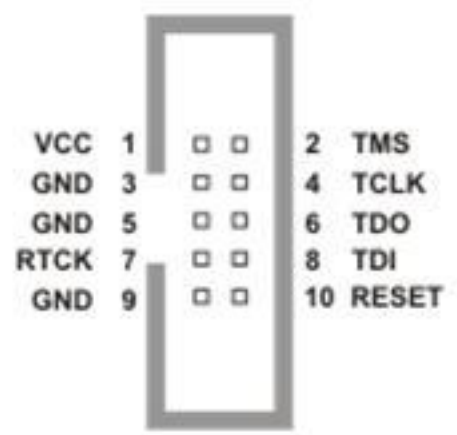
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 MICRO SD CONNECTOR		REV: 2.0	SHEET 14 OF 28

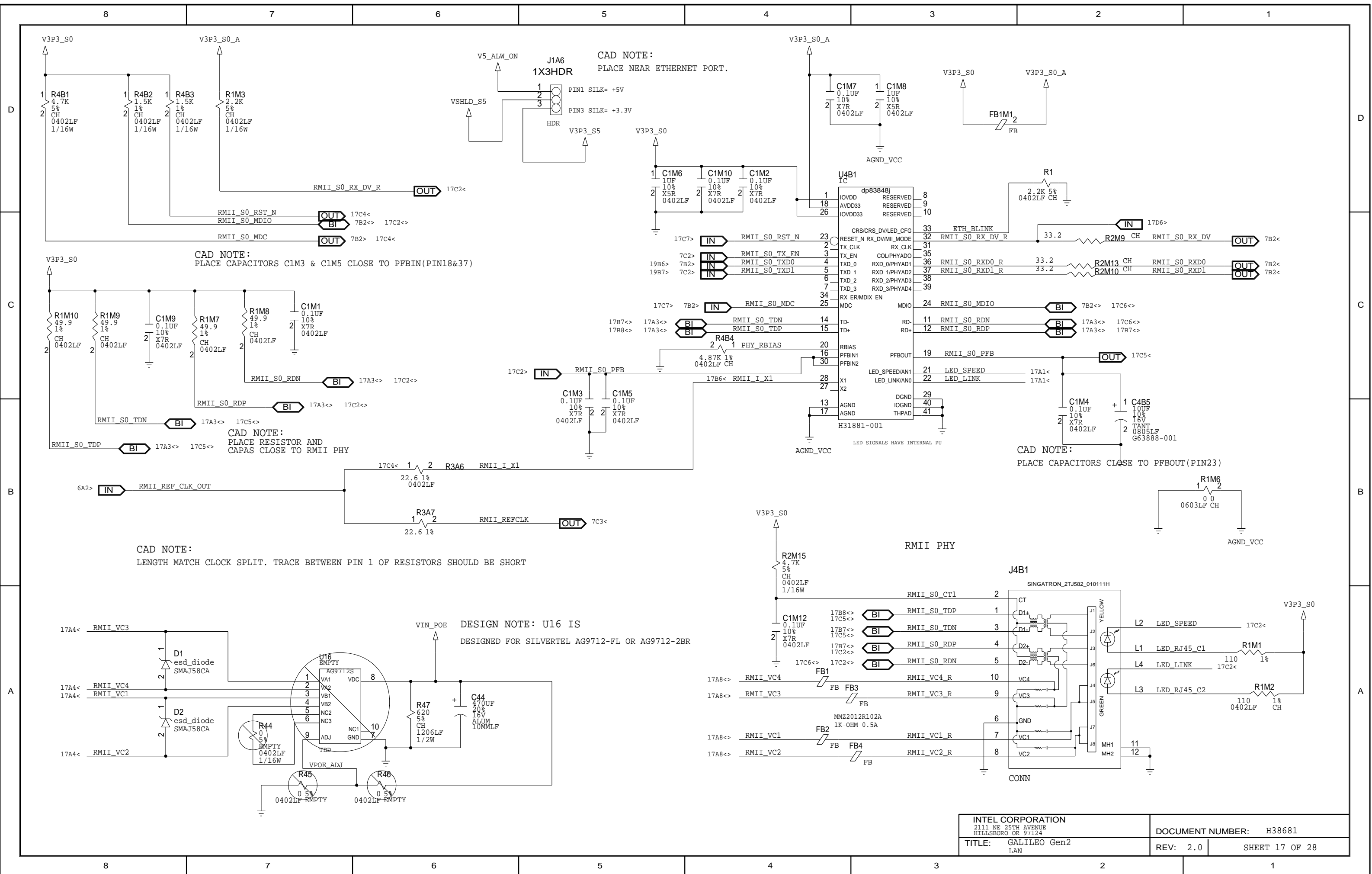




CAD NOTE:
PLACE CONNECTOR ON SOLDER-SIDE.

MINI-JTAG CONNECTOR





CAD NOTE:
PLACE NEAR ETHERNET PORT.

CAD NOTE:
PLACE CAPACITORS C1M3 & C1M5 CLOSE TO PFBIN(PIN18&37)

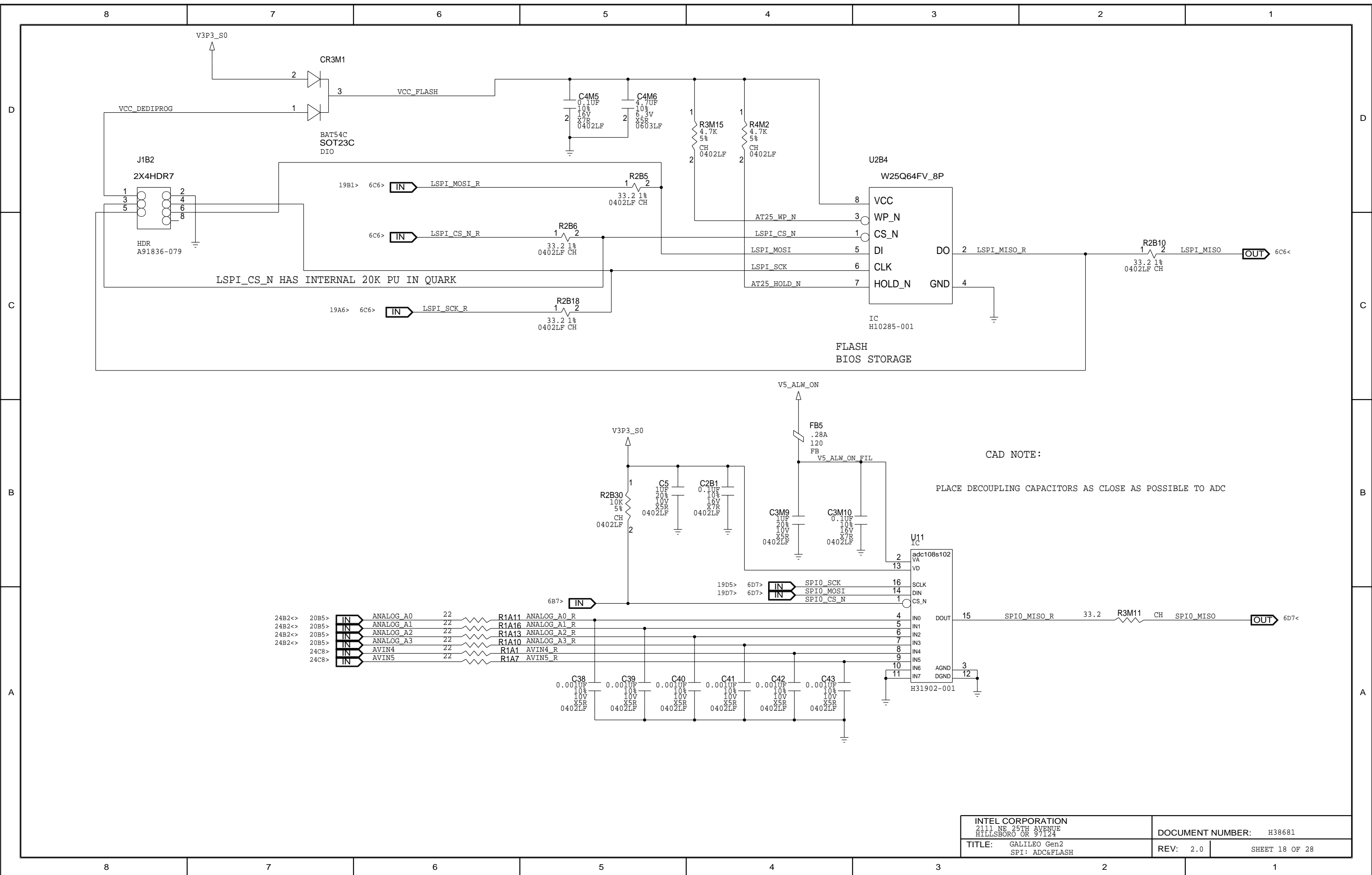
CAD NOTE:
PLACE RESISTOR AND CAPAS CLOSE TO RMIi PHY

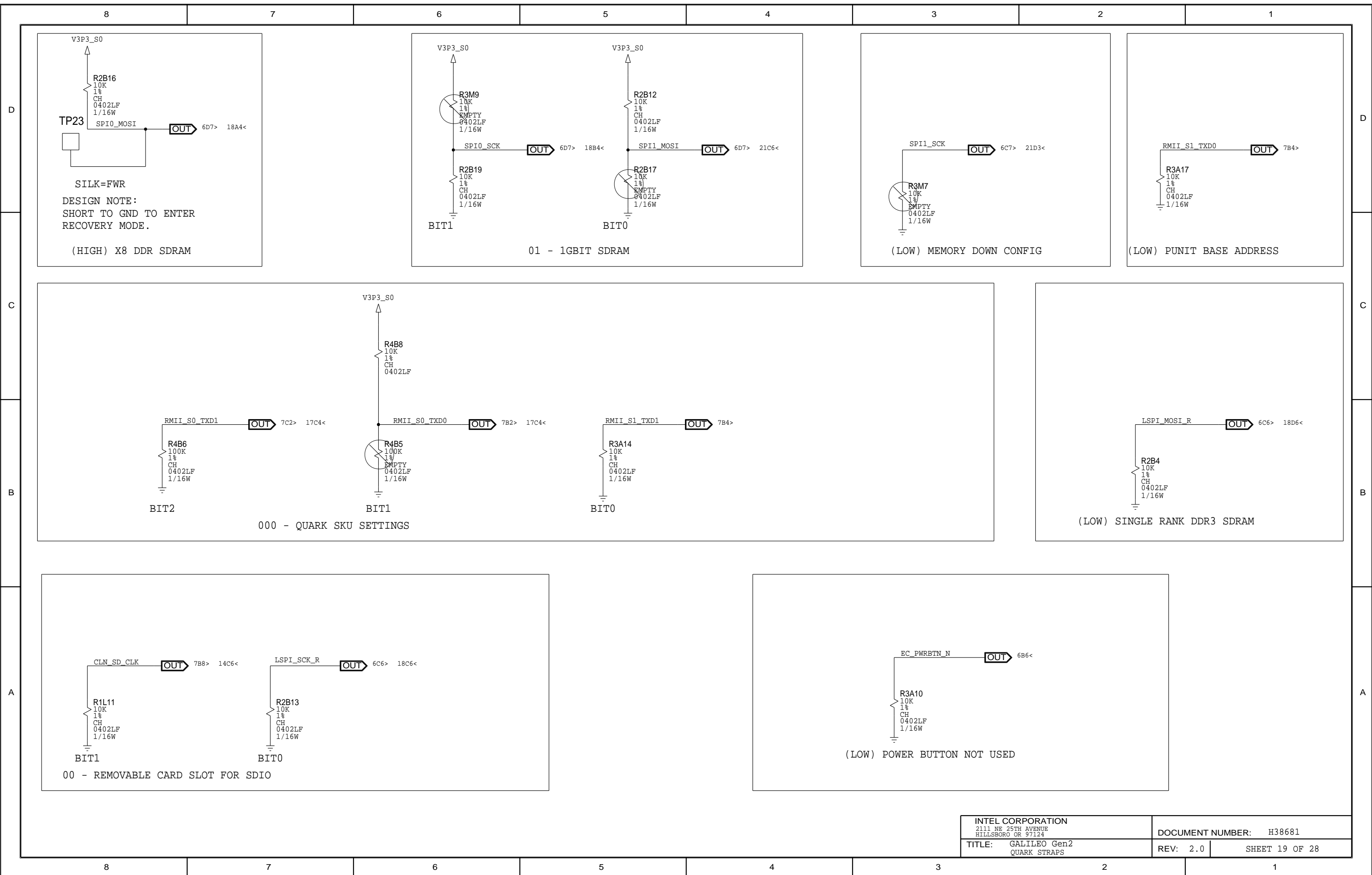
CAD NOTE:
PLACE CAPACITORS CLGSE TO PFBOUT(PIN23)

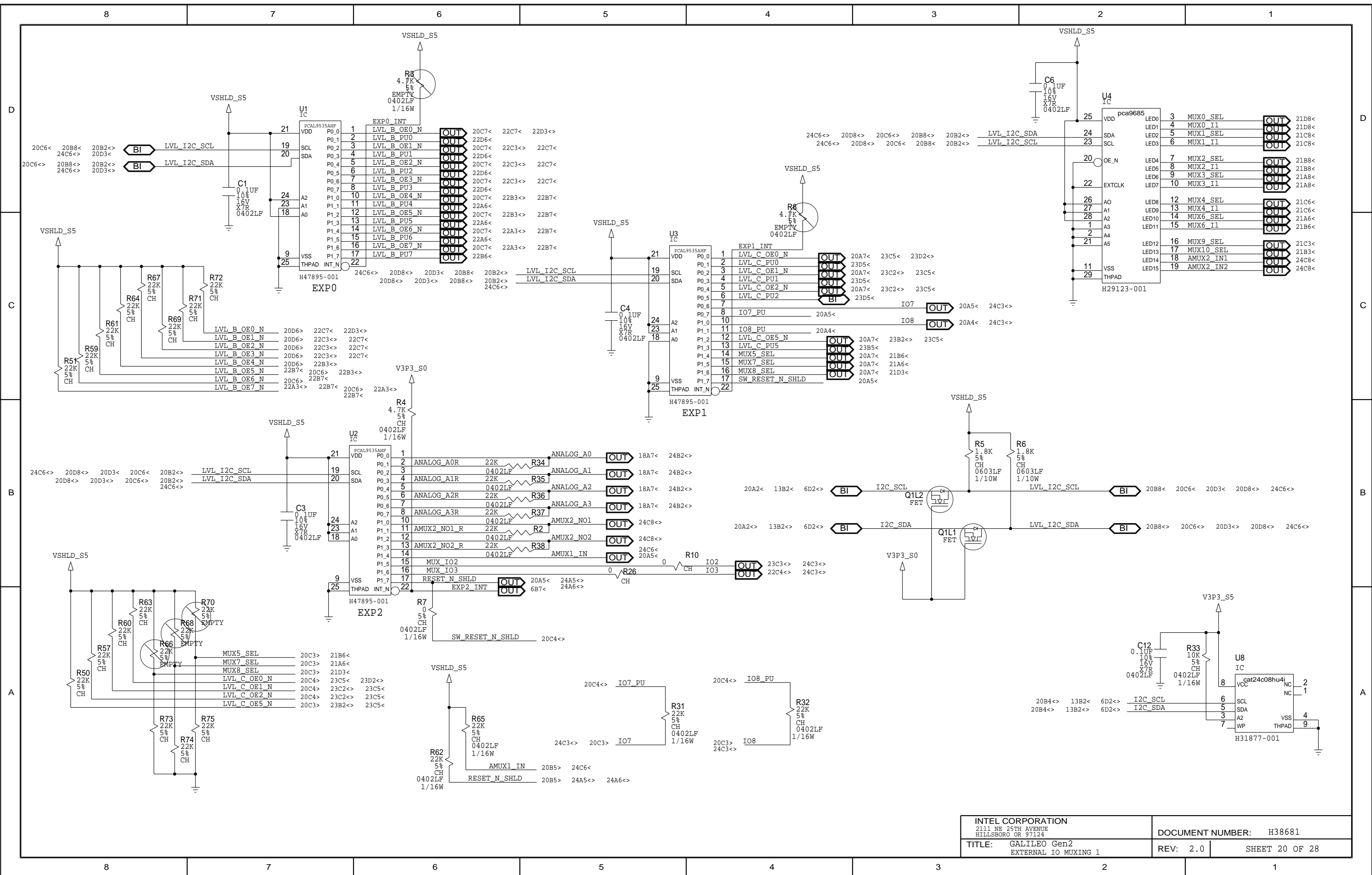
CAD NOTE:
LENGTH MATCH CLOCK SPLIT. TRACE BETWEEN PIN 1 OF RESISTORS SHOULD BE SHORT

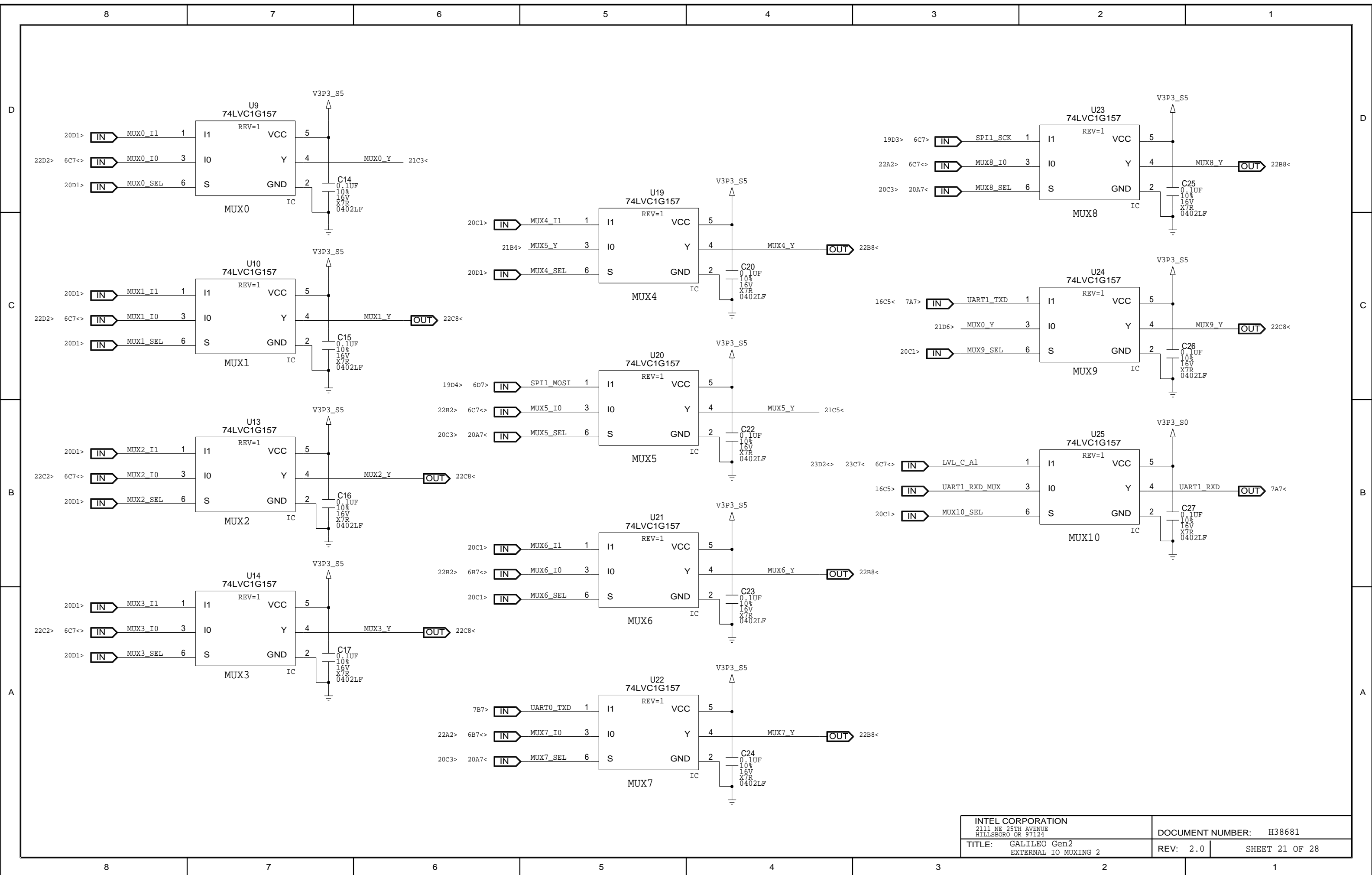
DESIGN NOTE: U16 IS
DESIGNED FOR SILVERTEL AG9712-FL OR AG9712-2BR

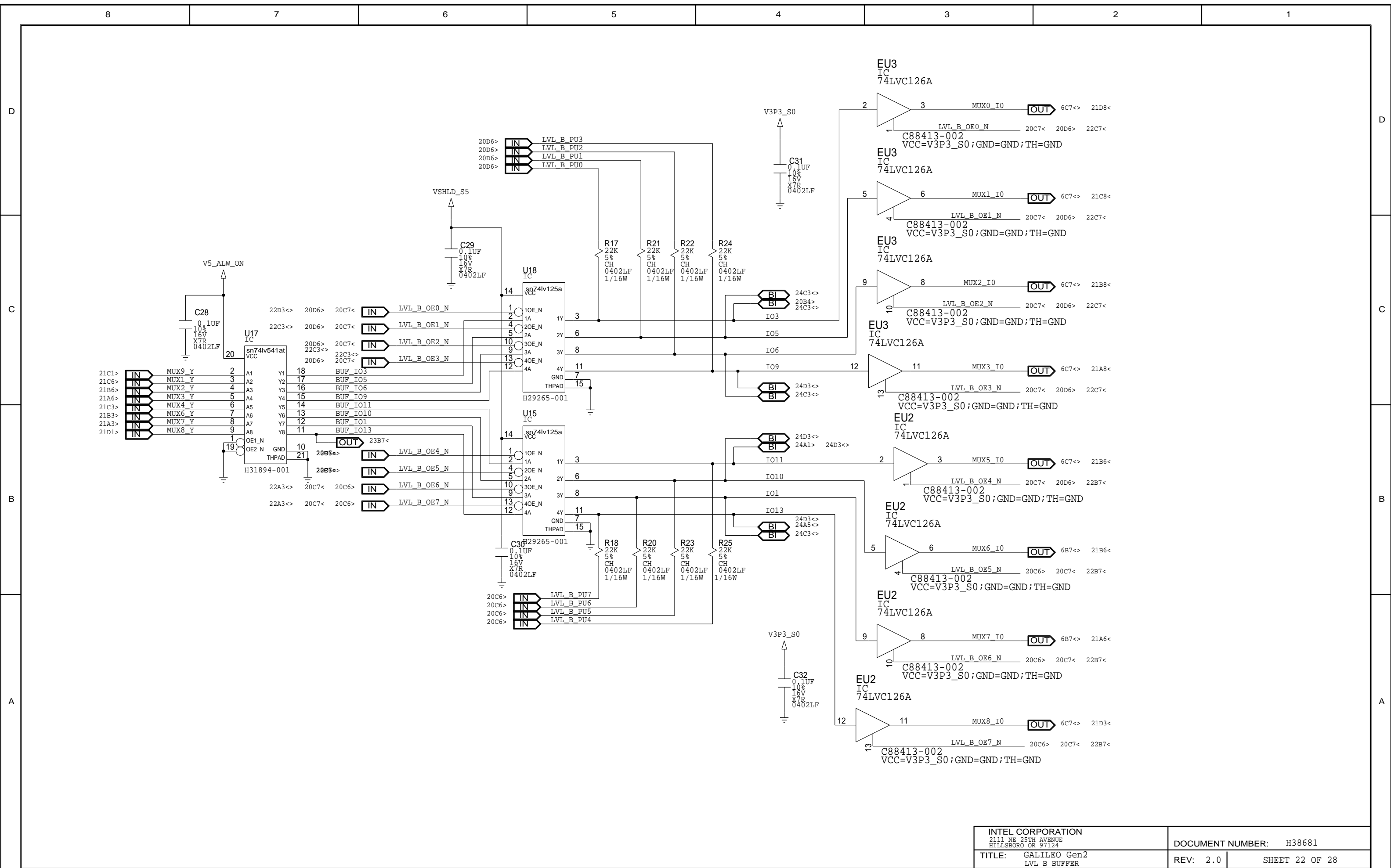
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 LAN		REV: 2.0	SHEET 17 OF 28

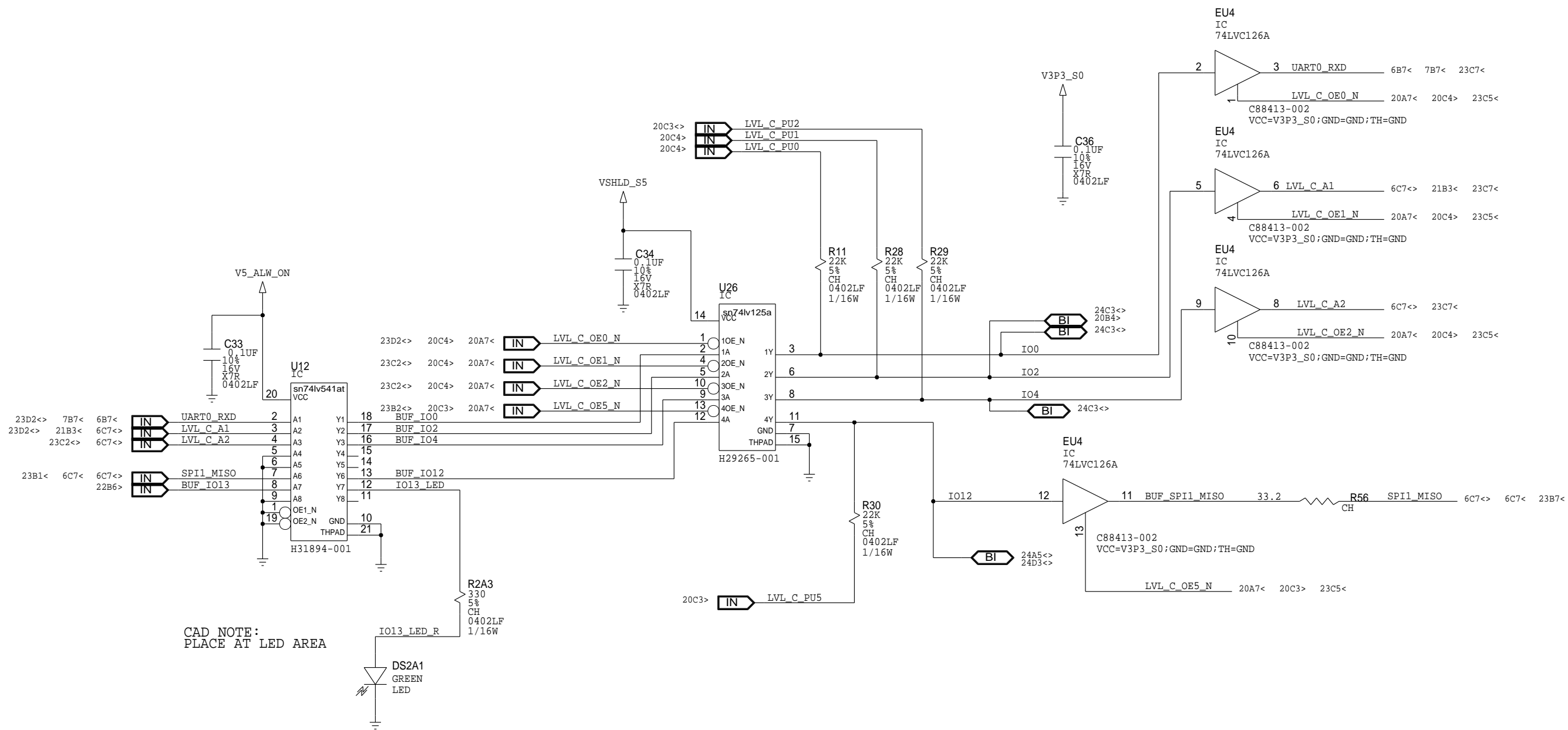




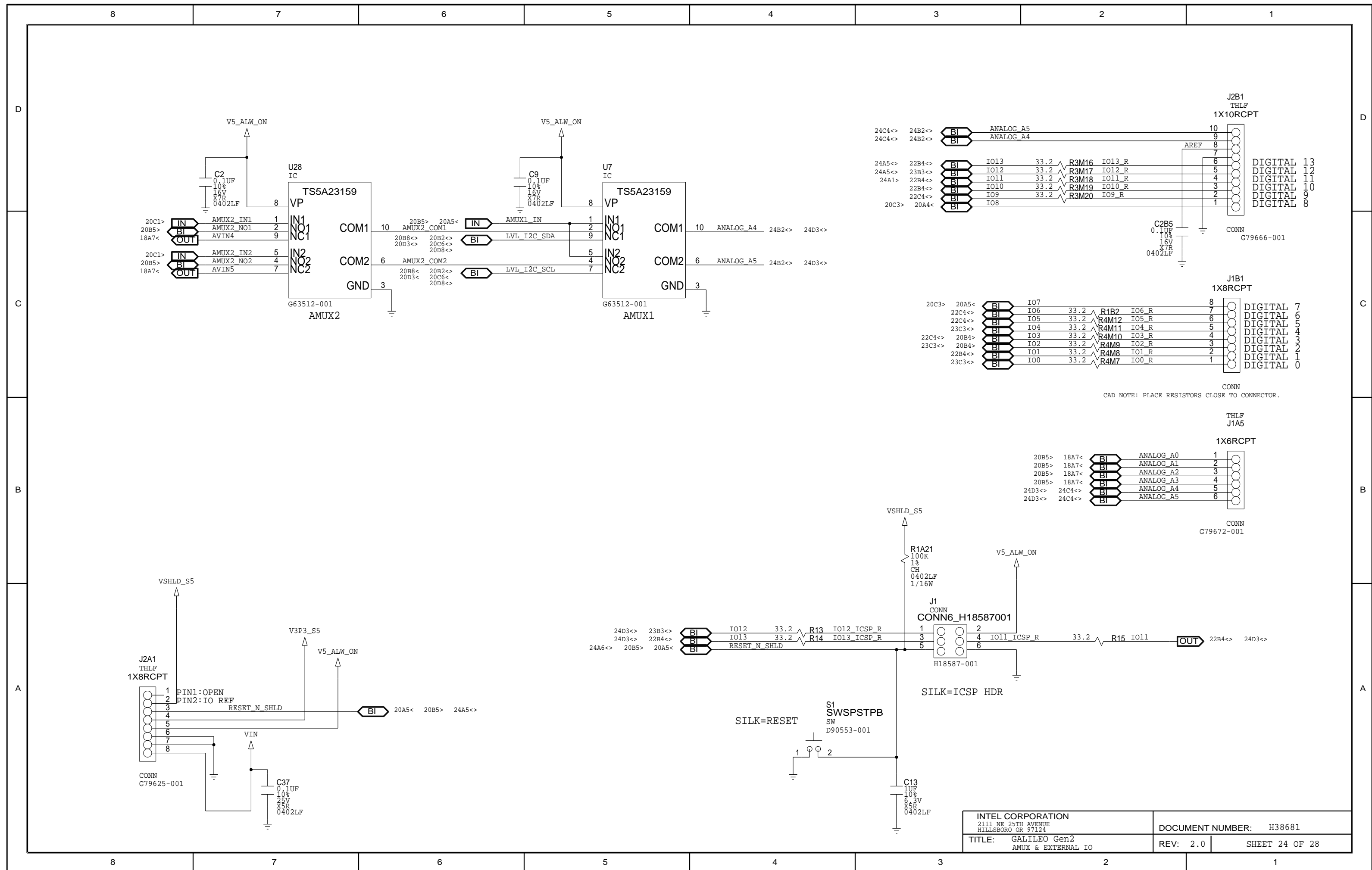


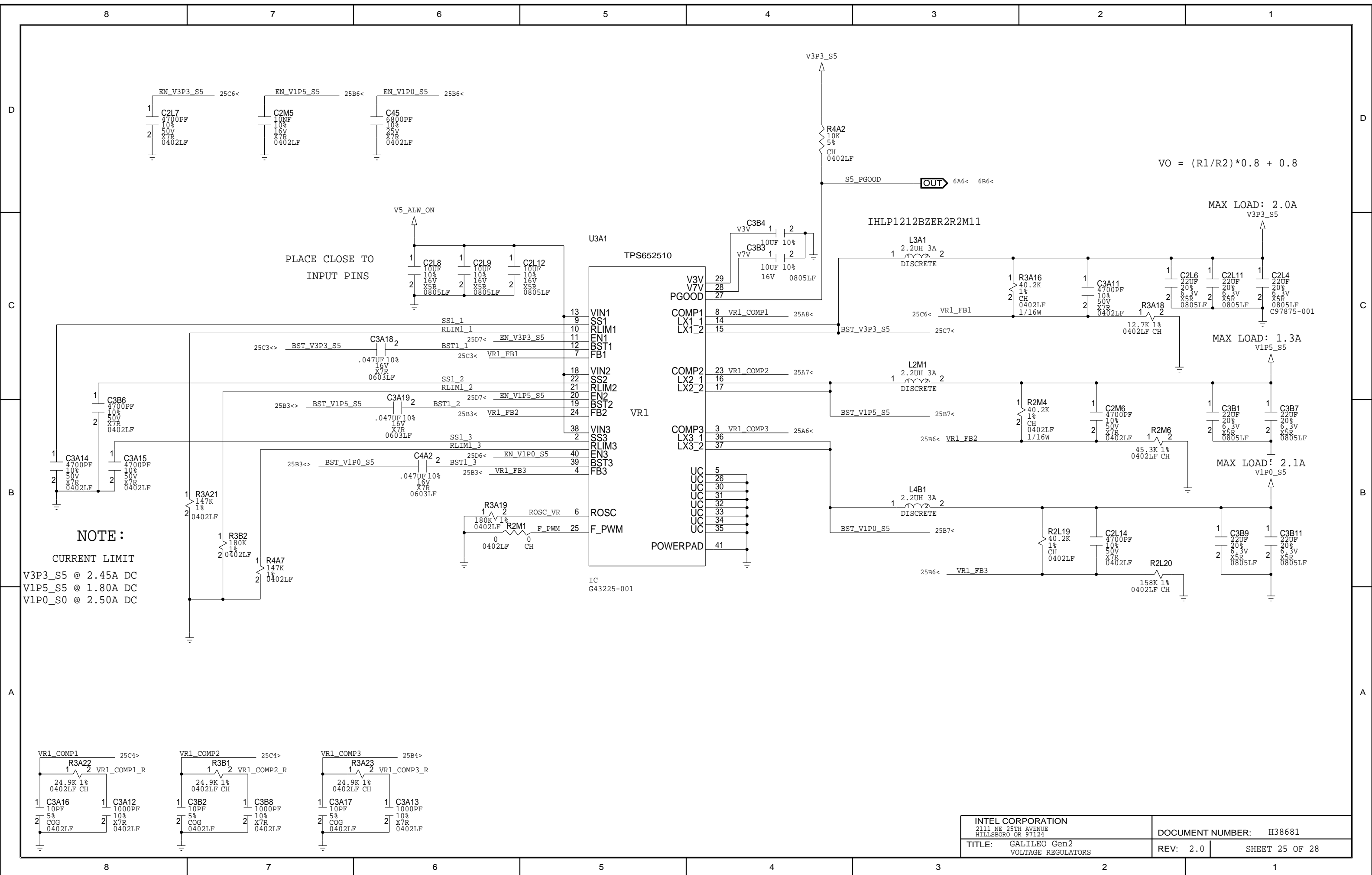






INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 LVL C BUFFER		REV: 2.0	SHEET 23 OF 28





PLACE CLOSE TO
INPUT PINS

$$VO = (R1/R2) * 0.8 + 0.8$$

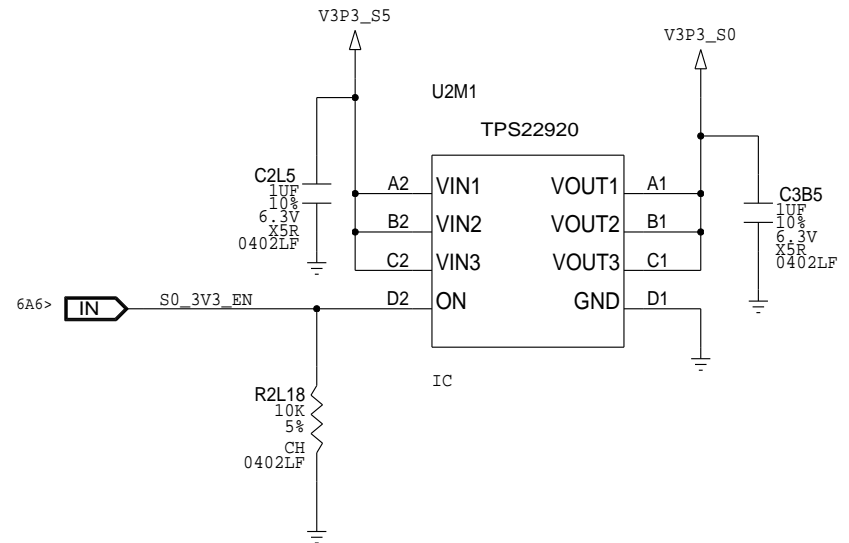
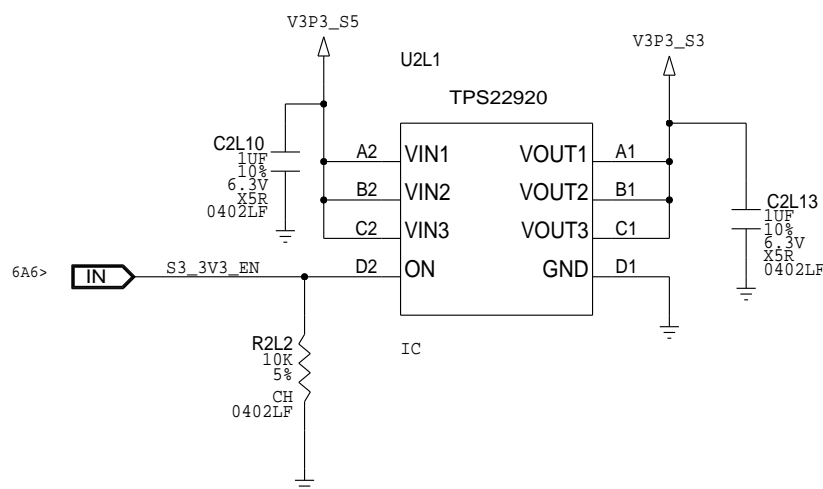
NOTE :

CURRENT LIMIT
V3P3_S5 @ 2.45A DC
V1P5_S5 @ 1.80A DC
V1P0_S5 @ 2.50A DC

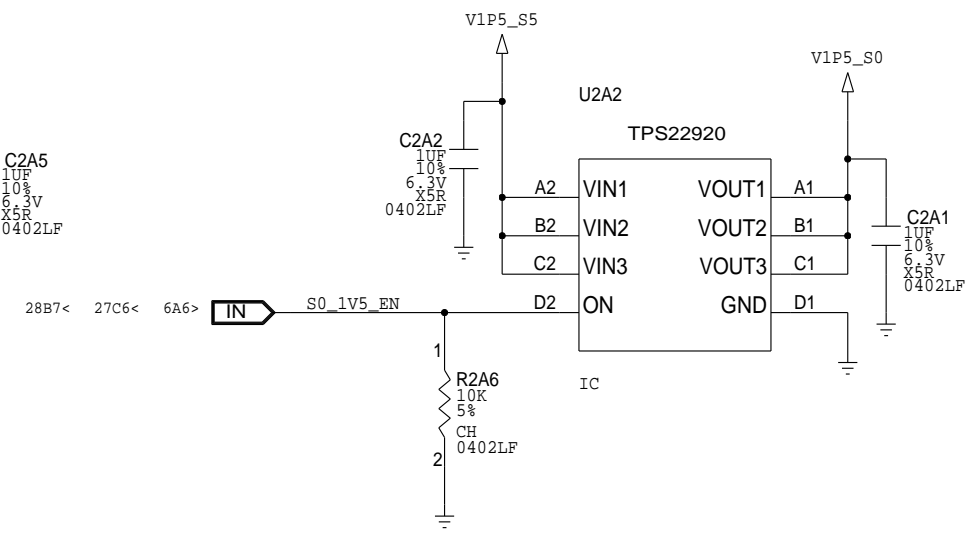
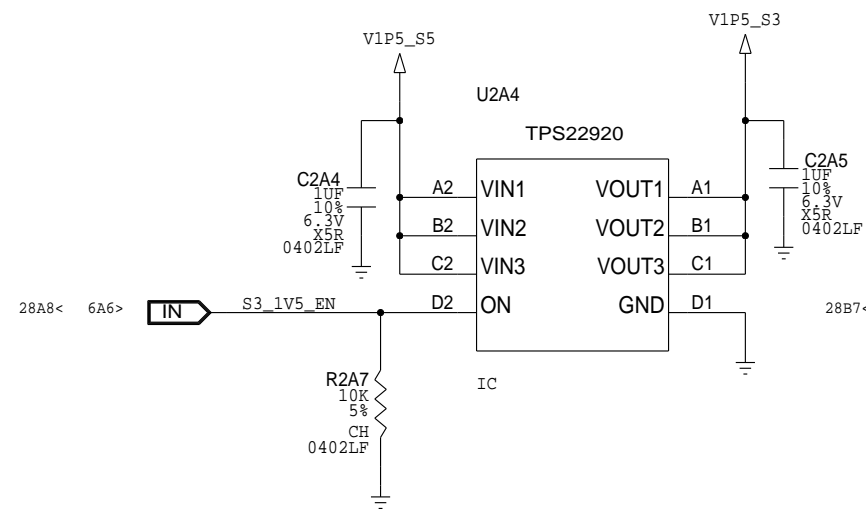
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 VOLTAGE REGULATORS		REV: 2.0	SHEET 25 OF 28

8 7 6 5 4 3 2 1

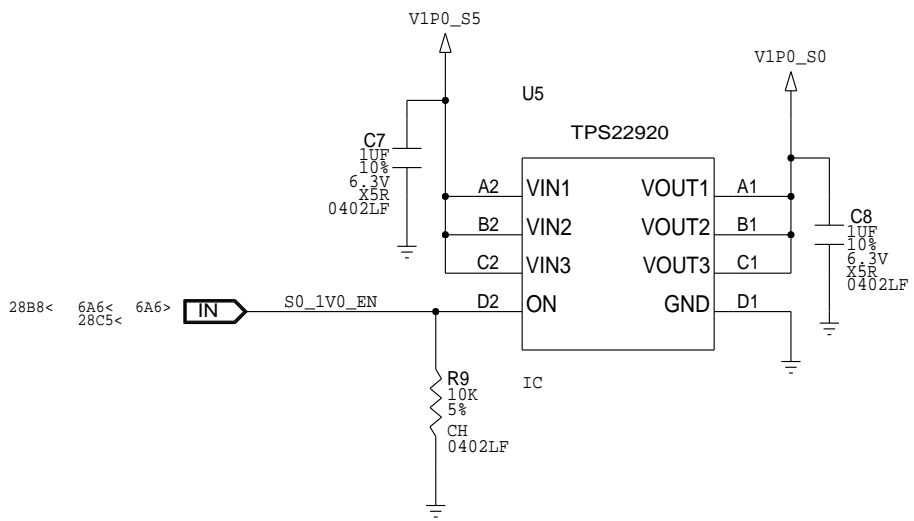
V3P3_S5 IS GENERATED W ON-BRD REGULATOR



V1P5_S5 IS GENERATED W ON-BRD REGULATOR



V1P0_S5 IS GENERATED W ON-BRD REGULATOR

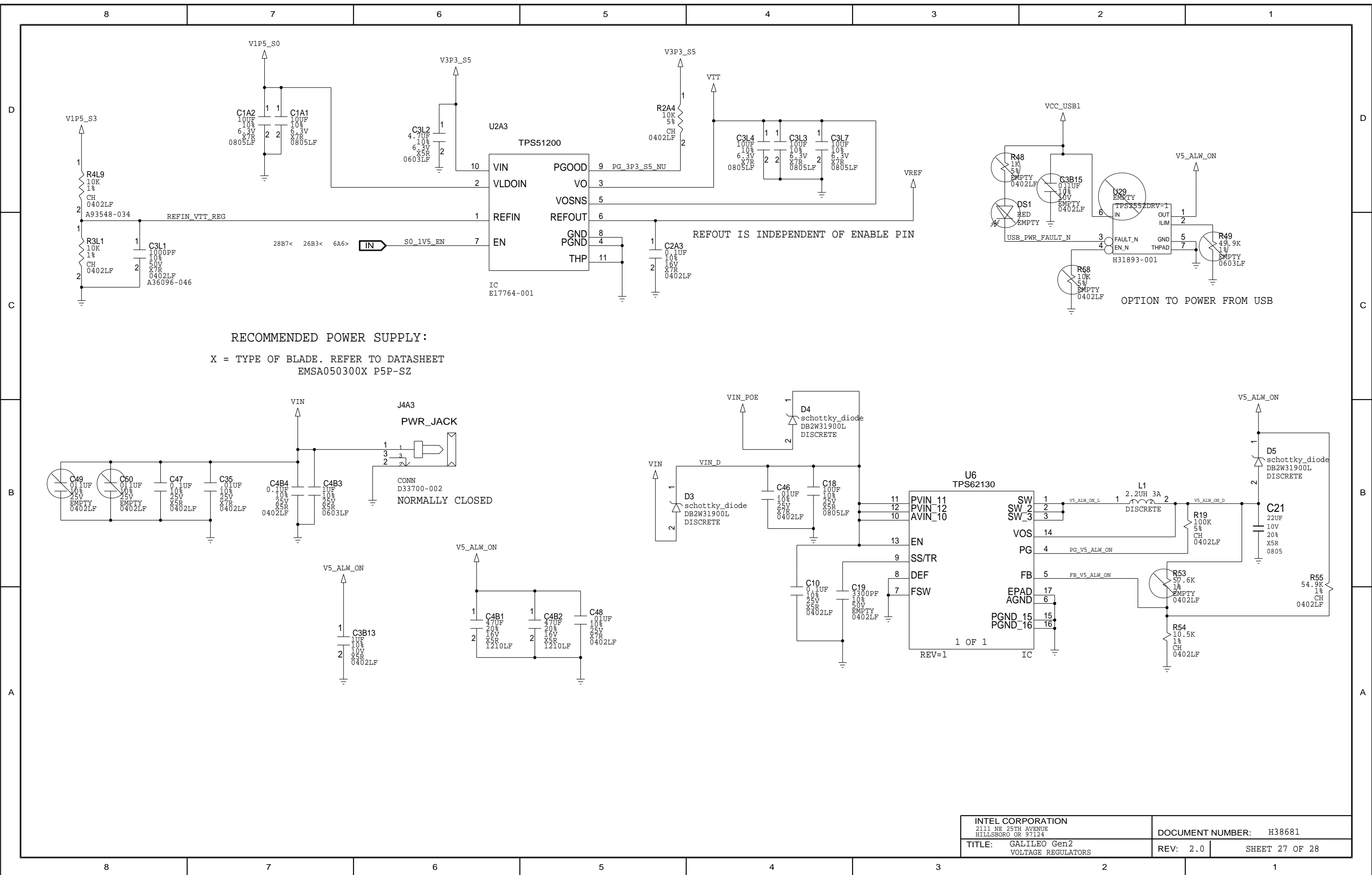


V1P0_S3 IS GENERATED INTERNALLY

V1P0_S0 IS GENERATED W ON-BRD REGULATOR

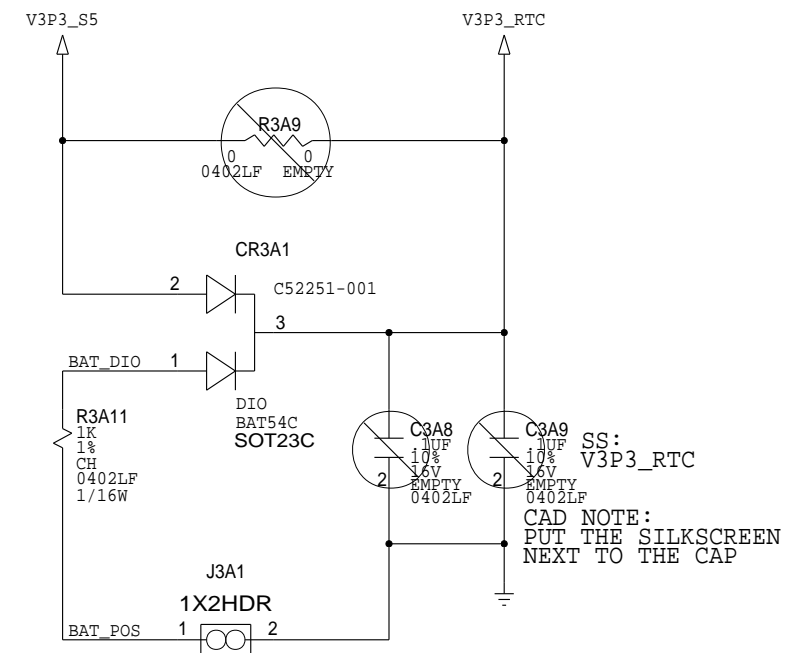
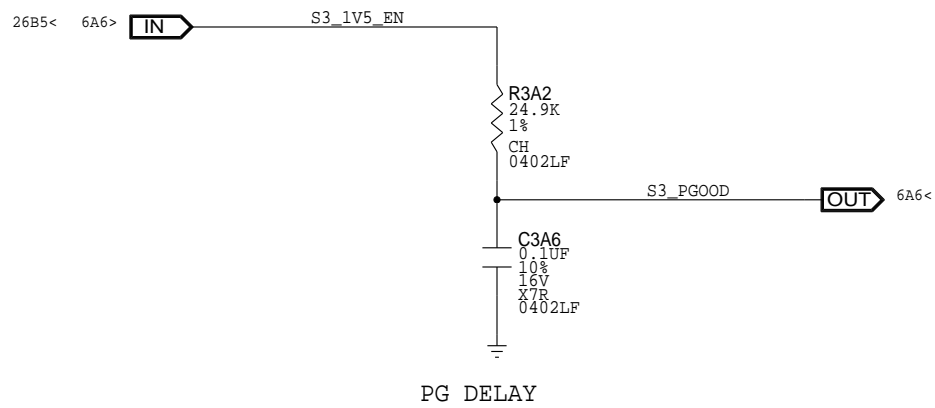
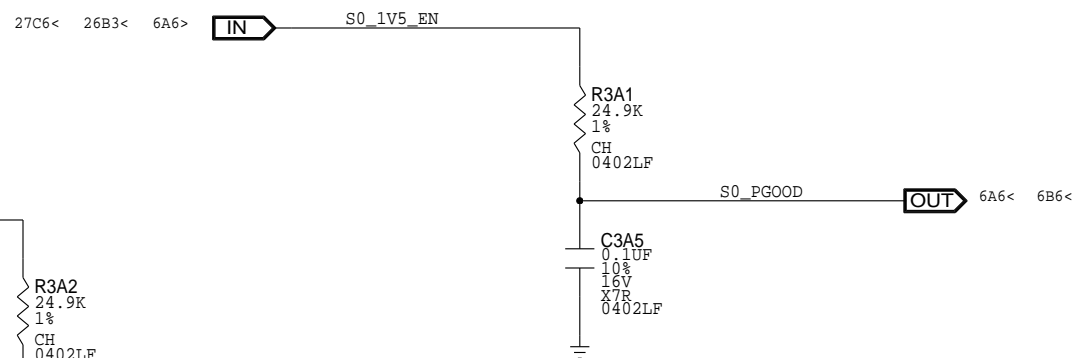
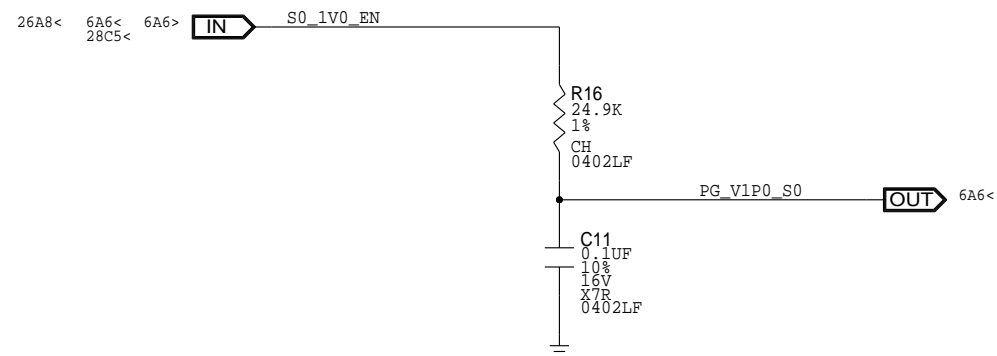
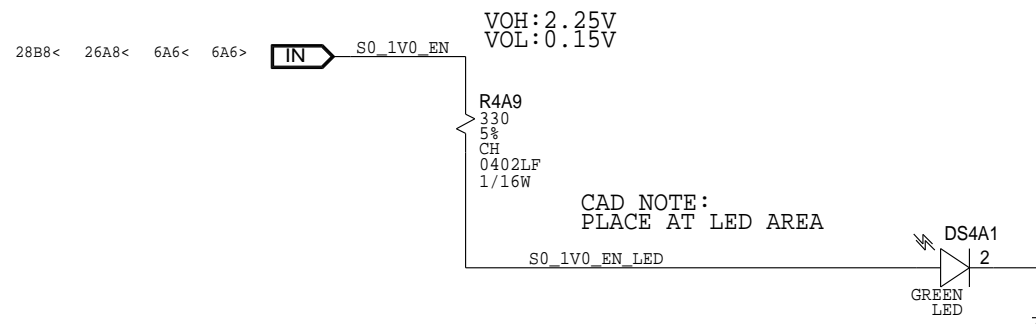
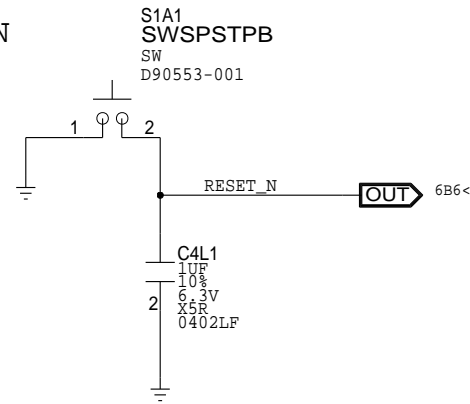
CAD NOTE:
PLACE DECOUPLING CAPS AS CLOSE AS POSSIBLE TO SWITCH PINS

8 7 6 5 4 3 2 1



NOTE: RESET_N HAS AN INTERNAL PU TO V3P3_S3

SS:
REBOOT BUTTON



CAD NOTE:
HDR
LABEL "+" AND "-" TERMINALS ON 2 PIN HDR
OFF-BOARD BATTERY

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 POWER BUTTONS & MISC		REV: 2.0	SHEET 28 OF 28